AMENDMENT TO CLAIMS

In the Claims

Please **AMEND** claims 1, 3, 4, and 7-16 as follows.

Please **CANCEL** claim 2.

A copy of all pending claims and a status of the claims provided below.

1. (Currently Amended) A flat panel display, comprising:

a luminescent device; ~~and first and second transistors for driving the luminescent device, wherein the first and second transistors have different resistance values~~

a driving transistor for driving the luminescent device;

a switching transistor for switching on and off the driving transistor,

wherein the driving transistor has a higher resistance than the switching transistor.

2. (Cancelled).

3. (Currently Amended) The flat panel display according to claim 1, wherein [[a]] the driving transistor ~~having a higher resistance value in the first and second transistors~~ includes multiple gates, a semiconductor layer having the high concentration source/drain regions, and an offset region [[is]] formed on the semiconductor layer between the multiple gates.

4. (Currently Amended) The flat panel display according to claim 1, wherein [[a]] the driving transistor ~~having a higher resistance value in the first and second transistors~~ includes a gate electrode, high concentration source/drain regions formed on both sides of the gate electrode, and an offset region formed between the gate electrode and the drain region.

5. (Original) The flat panel display according to claim 3 or claim 4, wherein the offset region is a high resistance region comprised of a low concentration impurity region on which low concentration impurities having the same conductivity type as the high concentration source/drain regions are doped as a whole or partially doped, or a high resistance region comprised of an intrinsic region on which impurities are not doped.

6. (Original) The flat panel display according to claim 3 or claim 4, wherein the offset region is a high resistance region having a zigzag shape.

7. (Currently Amended) The flat panel display according to claim 1, wherein [[a]] the driving transistor ~~having a higher resistance value in the first and second transistors~~ includes high concentration source/drain regions having different geometrical structure to have different resistance values, and a region connected to the luminescent device in the high concentration source/drain regions has a higher resistance value compared with the other region in the high concentration source/drain regions.

8. (Currently Amended) The flat panel display according to claim 1, wherein [[a]] the driving transistor ~~having a higher resistance value in the first and second transistors~~ includes high concentration source/drain regions having different sizes to have different resistance values, and a region connected to the luminescent device in the high concentration source/drain regions has a smaller size compared with the other region in the high concentration source/drain regions.

9. (Currently Amended) The flat panel display according to claim 8, wherein the region connected to the luminescent device in the high concentration source/drain regions of the driving transistor has the same width and a longer length, or the same length and a narrower width compared with the other region in the high concentration source/drain regions.

10. (Currently Amended) A flat panel display comprising R, G and B unit pixels, wherein at least one unit pixel of the R, G and B unit pixels includes ~~at least two or more transistors, each having source/drain regions, wherein at least drain region in the source/drain regions of at least one transistor in the transistors has a resistance value different from at least o drain region of the other transistor~~ a driving transistor for driving the luminescent device and a switching transistor for switching on and off the driving transistor, each having source/drain regions, wherein the drain region of the driving transistor has a higher resistance value than the drain region of the switching transistor.

11. (Currently Amended). The flat panel display according to claim 10, wherein the drain region ~~regions~~ of the ~~at least one transistor and the other transistor have resistance values which are different from each other by doping concentration difference of the drain regions~~ driving transistor has a higher resistance value than the drain region of the switching transistor by doping concentration difference.

12. (Currently Amended) The flat panel display according to claim 11, wherein the drain region of the ~~at least one transistor is~~ driving transistor comprises a region which is the [[of]] same conductivity type as the drain region of the other transistor, and on which low concentration impurities are doped as a whole or partially, or comprises a region on which

impurities are not doped.

13. (Currently Amended) The flat panel display according to claim 10, wherein drain regions of the ~~at least one transistor and the another transistor have resistance values which are different from each other~~ driving transistor has a higher resistance value than the drain region of the switching transistor by shape difference of the drain regions.

14. (Currently Amended) The flat panel display according to claim 13, wherein the drain region of the ~~at least one~~ driving transistor is formed in a zigzag shape.

15. (Currently Amended) The flat panel display according to claim 13, wherein the drain region of ~~the at least one~~ driving transistor has the same width and a longer length, or the same length and a narrower width compared with the drain region of the ~~other~~ switching transistor.

16. (Currently Amended) The flat panel display according to claim 11 ~~or claim 13~~, wherein the drain region of the ~~at least one~~ driving transistor includes an offset region of high resistance.

17-23. (Cancelled)